Hall Ticket Number:

Code No. : 41514

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

B.E. (IT) IV Year I-Semester Main Examinations, December-2017

VLSI Design

Time: **3** hours Max. Marks: **70**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Part-A (10 × 2 = 20 Marks)

1. List the conditional statements used in Verilog.
2. Write about Timing Control used in Verilog.
3. Define threshold voltage and write the threshold voltages of nMOS and pMOS.
4. Design $f = \overline{a + bc}$ using CMOS.
5. Draw the layout of series and parallel connected FET.
6. Explain how doped silicon layers are created using ion implantation.
7. List out the lambda-based Design Rules for Polysilicon.
8. Illustrate Dependence of mid-point voltage V_M on Relative Aspect ratio (i.e. β_n/β_p) of CMOS inverter.
9. Write the Verilog code of a D flip flop.
10. Draw the logic gate diagram of a PLA.

Part-B (5 × 10 = 50 Marks)
(All bits carry equal marks)

11. a) Write about switch level modeling and write the Verilog switch level code for inverter
    b) Explain RTL modeling, write the Verilog code for 2:4 decoder using RTL modeling
12. a) Give RC model of a FET and Explain
    b) Demonstrate CMOS Bubble pushing using an example
13. a) List and explain the masking sequence
    b) Explain with a neat diagram Photolithography
14. a) Develop the equation of rise time and fall time delay.
    b) Discuss about delay minimization in inverter cascade
15. a) Explain the working of a carry look ahead adder and write the Verilog code of same
    b) With a neat diagram explain the working and various operating modes of a 1T DRAM
16. a) Briefly explain various Data types Supported by Verilog HDL with necessary syntax and examples
    b) Design an 8:1 multiplexer using Transmission Gate based 2:1 MUX.
17. Answer any ***two*** of the following:
    a) Describe the layers used to create a MOSFET
    b) Write about cell concepts and cell based design
    c) Construct EEPROM Using Floating gate nFET.

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